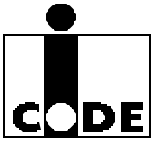
DATA SHEET



I•CODE1 Label ICs
Protocol Air Interface

Product Specification
Revision 1.6
Public

January 2005

Philips Semiconductors

PHILIPS

1 Contents

2 Definitions

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics section of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

2.1 Life Support Applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so on their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

2.2 Abbreviations

ASCII	American Standard Code for Information Interchange
CRC	Cyclic Redundancy Check
EAN	European Article Number
EAS	Electronic Article Surveillance
EEPROM	Electrically Erasable and Programmable Read Only Memory
EMI	Electromagnetic Interference
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
FFC	Film Frame Carrier
hex	Value in hexadecimal notation
IC	Integrated Circuit
ISM	Industrial, Scientific, Medical
LSB	Least Significant Bit or Byte
MSB	Most Significant Bit or Byte
RF	Radio Frequency
RZ	Return to Zero
SNR	Serial Number

3 Scope

This specification describes the RF communication protocol via air interface between I•CODE1 Label ICs and I•CODE read/write devices. It includes the physical layer (carrier frequency, modulation technique and bit-coding), and the protocol layer.

Based on this document a company which has already experience in RF circuit design and signal-processing should be able to design read/write devices for the I•CODE system.

4 Functional Description

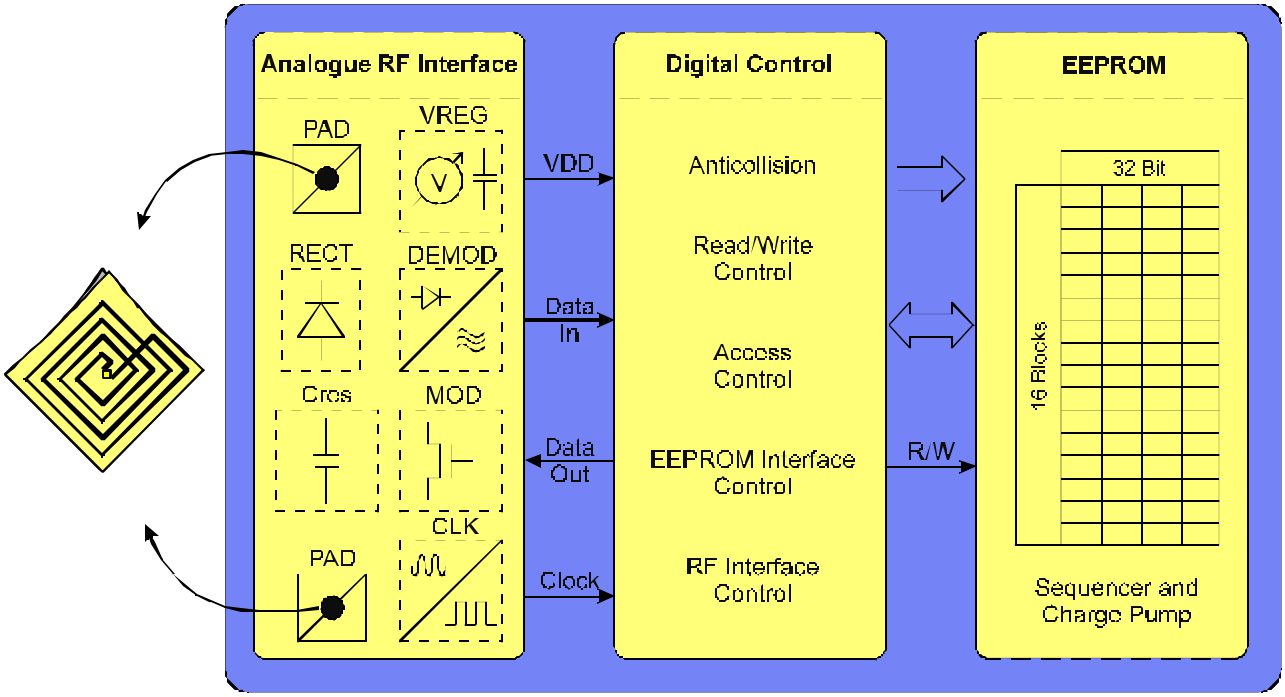
4.1 Basic Features

The I•CODE1 Label IC is a dedicated 512 bit memory chip for intelligent label applications like logistics and retail (including EAS) as well as baggage and parcel identification in airline business and mail services.

The I•CODE system offers the possibility of operating labels simultaneously in the field of the read/write device antenna (capability to resolve *Anticollisions*). It is designed for long range applications.

Whenever connected to a very simple and cheap type of antenna (as a result of the 13.56 MHz carrier frequency) made out of a few windings printed, winded, etched or punched coil the I•CODE1 Label IC can be operated without line of sight up to a distance of 1.5 m (gate width).

4.2 Block Diagram of the IC



The label requires no internal power supply. Its contactless interface generates the power supply and the system clock via the resonant circuitry by inductive coupling to the read/write device. The RF interface circuitry also demodulates data that are transmitted from the read/write device to the I•CODE Label, and modulates the electromagnetic field for data transmission from the I•CODE Label to the read/write device.

Data are stored in a non-volatile memory (EEPROM). The EEPROM has a memory capacity of 512 bit and is organised in 16 blocks consisting of 4 bytes each (1 block = 32 bits). The higher 12 blocks contain user data and the lowest 4 blocks contain the serial number, the write access conditions and some configuration bits.

4.3 Memory Organisation

The 512 bit EEPROM memory is divided into 16 blocks. A block is the smallest access unit. Each block consists of 4 bytes (1 block = 32 bits). Bit 0 in each byte represents the least significant bit (LSB) and bit 7 the most significant bit (MSB), respectively.

	Byte 0	Byte 1	Byte 2	Byte 3	
Block 0	SNR0	SNR1	SNR2	SNR3	Serial Number (lower bytes)
Block 1	SNR4	SNR5	SNR6	SNR7	Serial Number (higher bytes)
Block 2	F0	FF	FF	FF	Write Access Conditions
Block 3	x	x	x	x	Special Functions (EAS/QUIET)
Block 4	x	x	x	x	Family Code/Application Identifier/User Data
Block 5	x	x	x	x	User Data
Block 6	x	x	x	x	:
Block 7	x	x	x	x	:
Block 8	x	x	x	x	:
Block 9	x	x	x	x	:
Block 10	x	x	x	x	:
Block 11	x	x	x	x	:
Block 12	x	x	x	x	:
Block 13	x	x	x	x	:
Block 14	x	x	x	x	:
Block 15	x	x	x	x	User Data

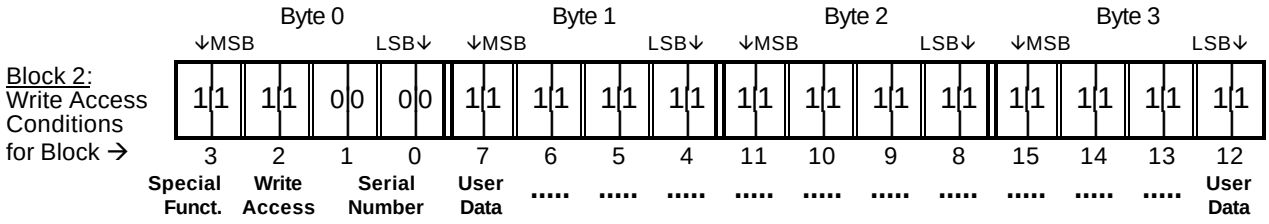
The values (in hexadecimal notation) shown in the table above are stored in the EEPROM after the wafer production process. The contents of blocks marked with 'x' in the table are **not** defined at delivery.

4.3.1 Serial Number

The unique 64 bit serial number is stored in blocks 0 and 1 and is programmed during the production process. SNR0 in the table represents the least significant byte and SNR7 the most significant byte, respectively.

4.3.2 Write Access Conditions

The Write Access Condition bits in block 2 determine the write access conditions for each of the 16 blocks. These bits can be set only to 0 (and never be changed to 1), i.e. already write protected blocks can never be written to from this moment on. This is also true for block 2. If this block is set into write protected state by clearing of bits 4 and 5 at byte 0, no further changes in write access conditions are possible.



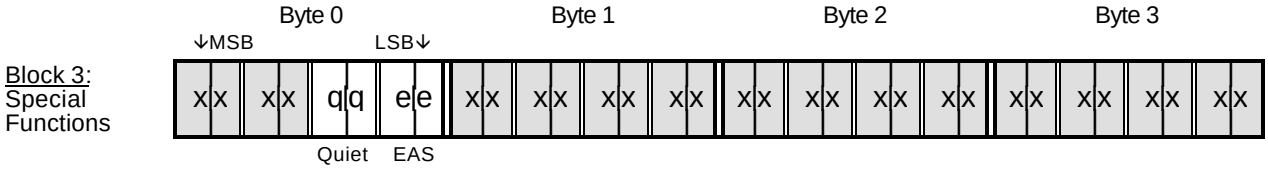
The ones in the 16 pairs of bits have to be cleared together if the corresponding block is wanted to be write protected forever (1|1 → write access enabled, 0|0 → write access disabled). Writing of bit pairs 1|0 or 0|1 to block 2 is not allowed!

It is extremely important to be particularly careful when clearing the Write Access bits in block 2, as you can lose write access to all of the blocks on the label in case of a mistake. Of course you can use this feature to put the label into a hardware write protected state!

4.3.3 Special Functions (EAS/QUIET)

The Special Functions block holds the two EAS bits (Electronic Article Surveillance mode active → the label answers at an EAS command) as well as the two QUIET bits (QUIET mode enabled → the label is permanently disabled but can be activated again with the 'Reset QUIET bit' command). The state of QUIET mode does **not** influence the functionality of the EAS command.

The remaining 28 bits (greyed 'x' in the following figure) are reserved for future use.



Quiet: q|q = 1|1 → QUIET mode enabled q|q = 0|0 → QUIET mode disabled
EAS: e|e = 1|1 → EAS mode enabled e|e = 0|0 → EAS mode disabled

Writing of bit pairs 1|0 or 0|1 to block 3 is not allowed!

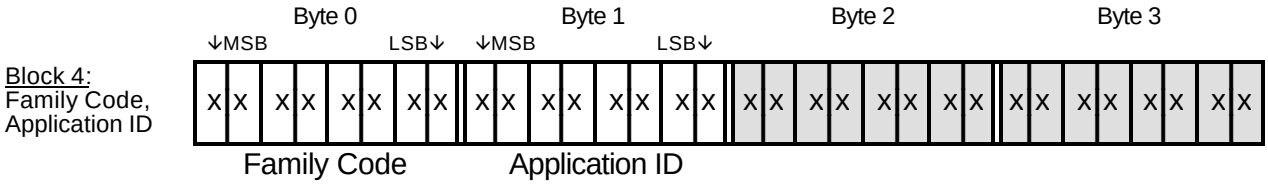
Changing of the Write Access Control or Configuration must be done in secure environment (by reading the current value of the block and masking in the new values for bit positions that may be changed). The label must not be moved out of the communication field of the antenna during writing! We recommend to put the label close to the antenna and not to remove it during operation.

4.3.4 Family Code and Application Identifier

The I•CODE system offers the feature to use (independently) Family Codes and/or Application Identifiers with some commands (this ability can be used to create 'label families').

These two 8-bit values are located at the beginning of User Data (block 4) as shown in the following figure and are only evaluated if the corresponding bytes at the commands are unequal to zero.

Only if both corresponding parameter bytes at the commands Anticollision/Select, Unselected Read and EAS, respectively, are set to zero, block 4 can be used for user data without restriction.



The greyed bytes are for customer usage as well as the remaining blocks (5 to 15) are.

4.4 Configuration of delivered ICs

I•CODE1 Label ICs are delivered with the following configuration by Philips:

- Serial number is unique and read only
- Write Access Conditions allow to change all blocks (with the exception of both serial number blocks)
- Status of EAS mode is **not** defined
- Status of QUIET mode is **not** defined
- Family Code and Application Identifier are **not** defined
- User Data memory is **not** defined

NOTE: As the status of QUIET mode is not defined at delivery, the first command to be executed on the I•CODE1 Label IC should be the Reset QUIET Bit command!

NOTE: Due to the fact that the EAS mode is undefined at delivery, the EAS MODE shall be set (enable or disable) according to your application requirements during the test or initialisation phase.

5 I•CODE System and Radiation Restrictions

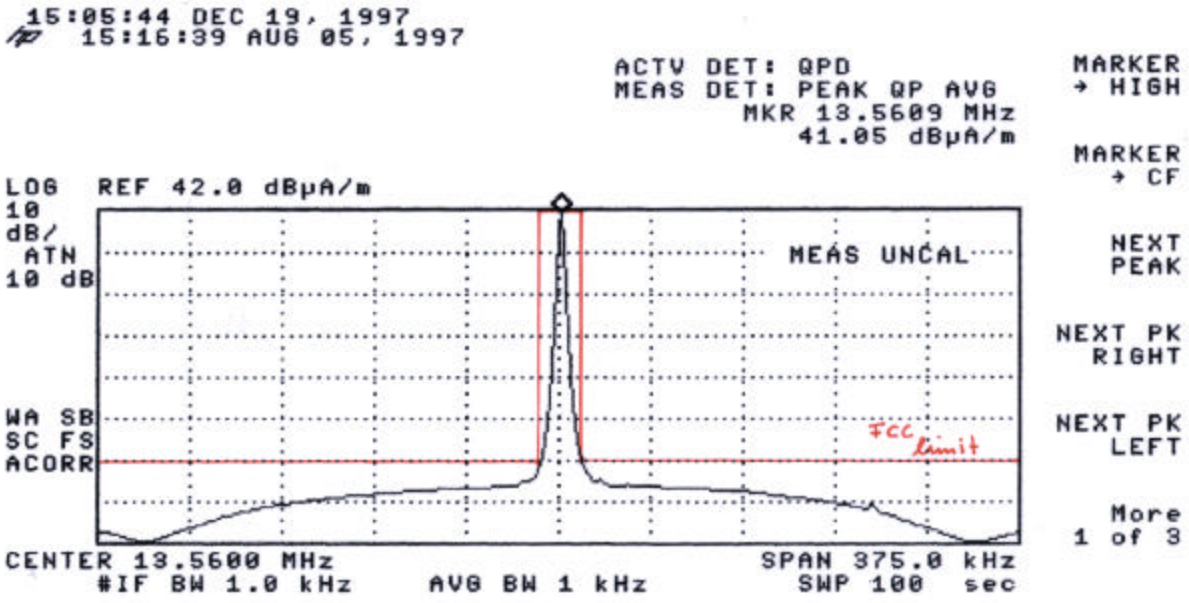
A main limitation for the achievable read/write distance of passive systems is the radiation limit concerning the carrier frequency and the side bands due to data transmission from the read/write device to the label.

For the carrier frequency the limit in the United States (FCC 47 part 15) is 10 000 µV/m at 30 m distance, in Europe (EN 300-330) the limit is 42 dBµA/m at 10 m distance, which is a little higher value.

The levels for the side bands in the United States are extremely low. Only 30 µV/m at 30 m distance are allowed. This means that the side bands have to be 50 dB lower than the carrier. In Europe the side bands (carrierfrequency +/- 150 kHz) have to be 33 dB lower than the carrier. For comparable systems this difference is only about 20 dB.

To comply with even the stringent FCC regulations the I•CODE system uses special techniques such as 10 % modulation of the carrier at the communication from the read/write device to the I•CODE Labels, special coding of the transmission data and also a special protocol. As a result the I•CODE system fulfils in the *standard mode* the strict FCC requirements with no limitation on the read/write distance caused by the side band levels.

A measurement at the I•CODE system working at standard mode is shown in the following plot, where also the FCC limits are marked:



Note: The reason for the FCC limit drawn at 60 dB is the used measurement band width of 1 kHz in contrast to 10 kHz, which results in the above mentioned 50 dB side band margin.

For short range operation with lower power from the transmitter or when using the I•CODE1 Label IC in regions where the radiation limits at the side band frequencies are higher, a so-called *fast mode* is implemented at the I•CODE1 Label IC. In principal this faster operating mode uses the same protocol as the standard mode, the only difference is the byte coding from the read/write device to the smart label.

6 RF Communication

The I•CODE1 Label IC supports bi-directional (read and write) communication based on 13.56 MHz carrier frequency. The operation of several I•CODE Labels at the same time in the antenna field is possible due to a specific *Anticollision* algorithm using so-called *timeslots*.

Note: All the timings given in this document are **nominal** values and are calculated as multiples of 4.72 µs (= 64 * 1/13.56 MHz).

6.1 Data Transmission from Read/Write Device to I•CODE Label (RX)

6.1.1 Modulation

The I•CODE1 Label IC works with a demodulator circuitry which is capable to detect an amplitude modulation of the carrier frequency of 10 %. Due to the signal shape caused by antennas with **high** quality factors (e.g. Q = 100) and tolerances of the on-chip demodulator the recommended modulation index seen at the I•CODE Label should be 14 % (according to data sheet 'I•CODE1 Label IC, Chip Specification').

The modulation index m is defined in the following way:

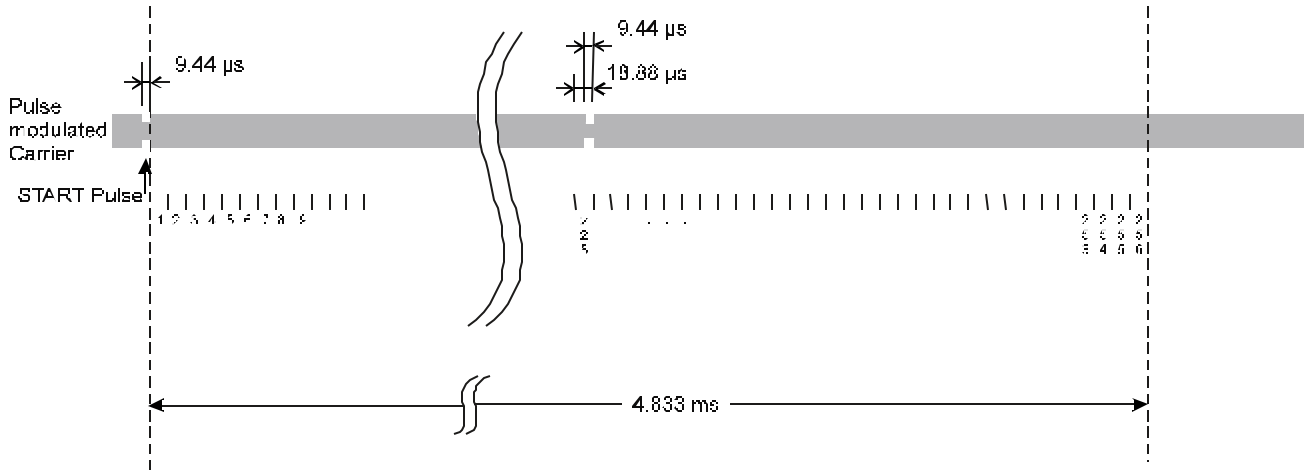
$$m = \frac{V_{max} - V_{min}}{V_{max} + V_{min}}$$

V_{max} ..... Voltage of RF carrier without modulation
V_{min} ..... Voltage of RF carrier during modulation

6.1.2 Bit Coding

6.1.2.1 Standard Mode

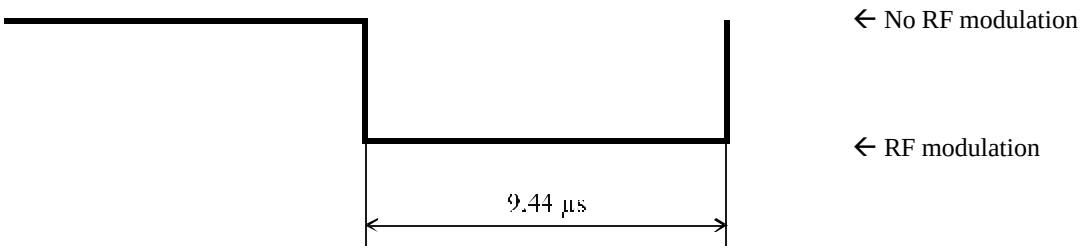
To keep the side band levels for long range operation in countries where the limits at these frequencies are very low (for example FCC regulations) within these limits, the RX data bytes are transmitted using a '1 out of 256' pulse position code.



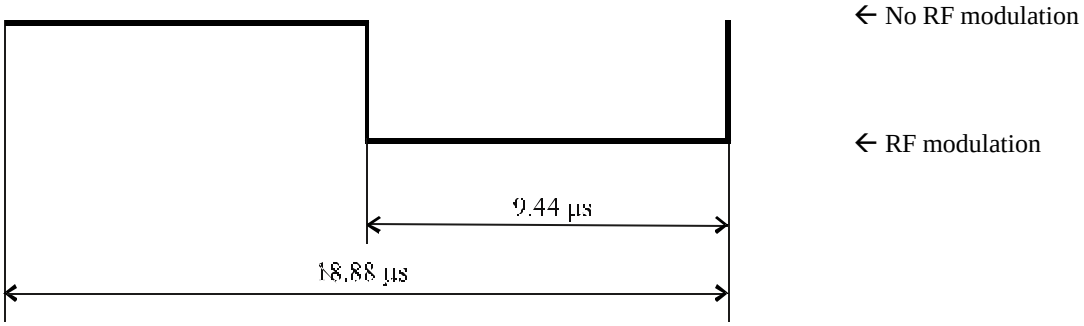
The above diagram illustrates the pulse position modulation technique. The position of a single pulse within a 256 position frame (each bit position has a duration of 18.88 µs, the actual modulation has to occur only during the second half of this bit frame) contains 1 byte (8 bit) information. The transmission of one byte takes 4.833 ms. The **first** byte is preceded by a start pulse, which is a modulation of 9.44 µs. This start pulse is transmitted only once at the beginning of each command.

In the example above RX data E1 hex (225 decimal) is received by the chip.

The start pulse for the standard mode is coded in the following way:



The pulse within one of the 256 bit positions is coded as follows:

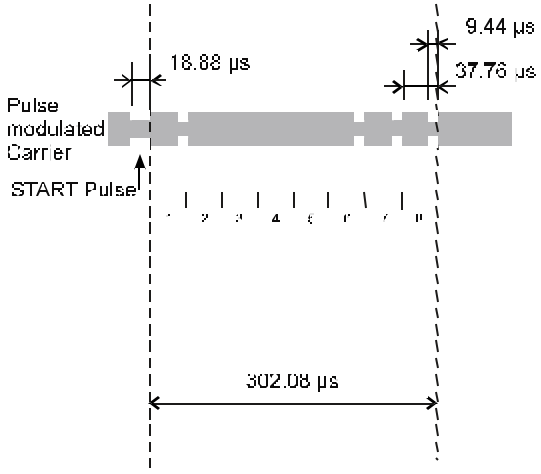


A zero-byte is transmitted by an unmodulated carrier during the whole 4833.28 µs byte frame.

Note: Pulse position 256 is not used for the transmission of a command byte.

6.1.2.2 Fast Mode

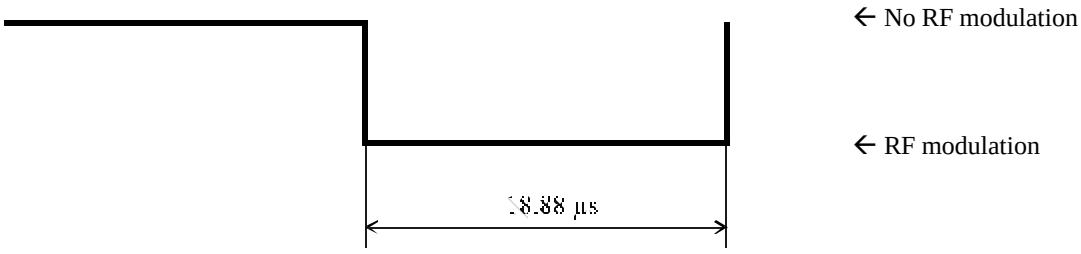
For short range operation with lower RF power or when using the I•CODE1 Label IC in countries where the radiation limits at the side band frequencies are higher, a so-called *fast mode*, which is also implemented, can be used. In principal this faster operating mode uses the same protocol as the standard mode. The only difference is the byte coding of the command sent to the label. Instead of the '1 out of 256' code an RZ code is used.



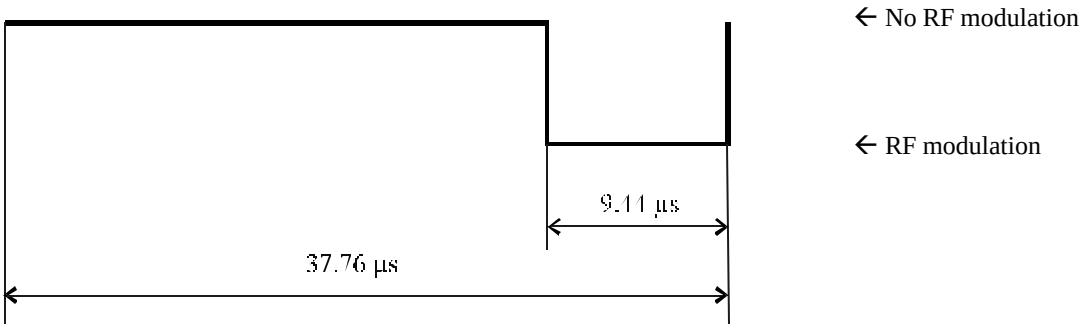
The above diagram illustrates the coding used in the fast mode. In this mode the coding is done bit per bit. In this example the same RX data E1 hex (225 decimal) is received by the chip.

The fast mode can be activated with a longer duration of the start pulse (nominal 18.88 µs) independently for every command. This start pulse is transmitted only once at the beginning of each command.

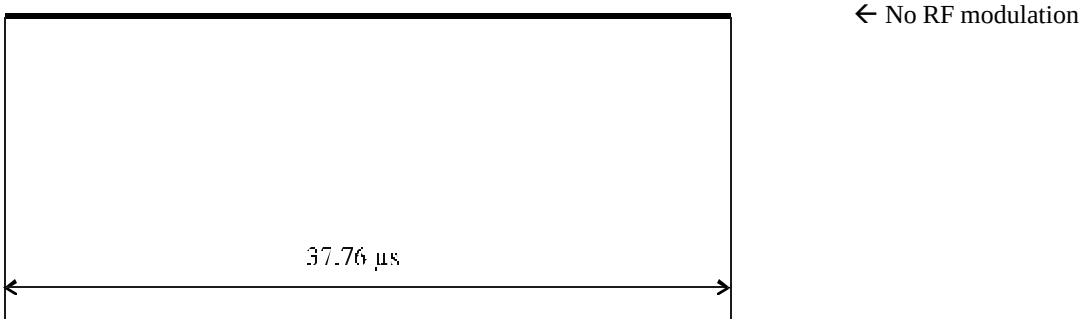
The start pulse for the fast mode is coded in the following way:



Each byte is started with the LSB, each of the 8 bits within a byte is coded as follows:



Logic 1 is transmitted by an unmodulated carrier during 28.32 µs and a modulated carrier during 9.44 µs.



Logic 0 is transmitted by an unmodulated carrier during the whole 37.76 µs bit frame.

This coding allows a high transmission speed of 26.5 kBaud in the direction from the read/write device to the I•CODE1 Label IC.

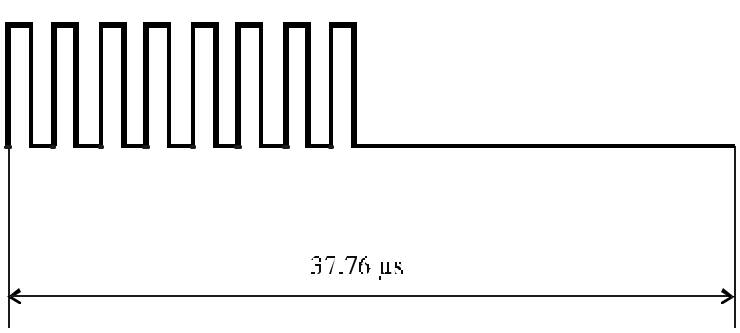
6.2 Data Transmission from I•CODE Label to Read/Write Device (TX)

6.2.1 Modulation

The 13.56 MHz carrier is load modulated with a 423.75 kHz sub-carrier which is Manchester-coded by a 26.5 kBaud data stream using the bit coding described in the following section:

6.2.2 Bit Coding

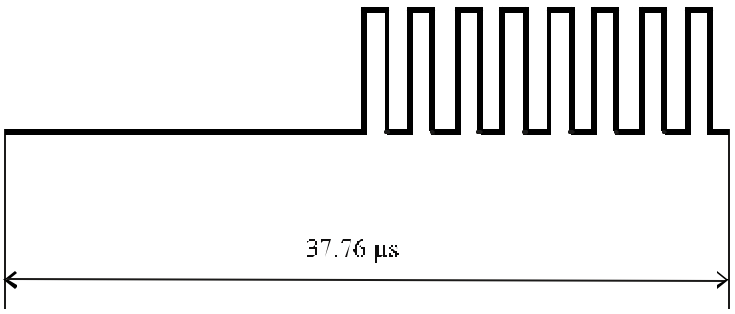
In the direction from the I•CODE1 Label IC to the read/write device the 13.56 MHz carrier is load modulated with the shown signals (sub-carrier frequency = 423.75 kHz):



← Load modulation with sub-carrier at the first half of the bit

← No load modulation at the second half of the bit

Logic 1

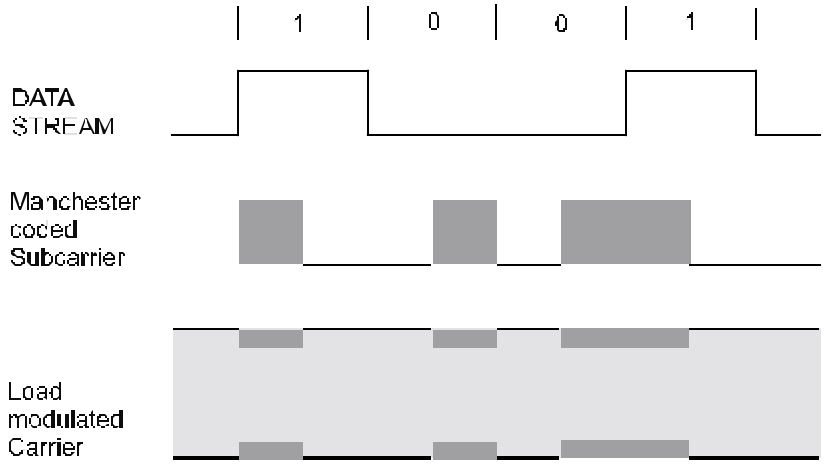


← Load modulation with sub-carrier at the second half of the bit

← No load modulation at the first half of the bit

Logic 0

The following figure shows an example of the data transmission from the I•CODE1 Label IC to the read/write device:



There is no difference in the response timing for standard and fast mode.

7 Communication Frames

All instruction bytes, parameters and CRC bytes from the read/write device as well as all responses from the I•CODE1 Label IC (serial number, read blocks, CRC bytes) are transmitted with the LSB first.

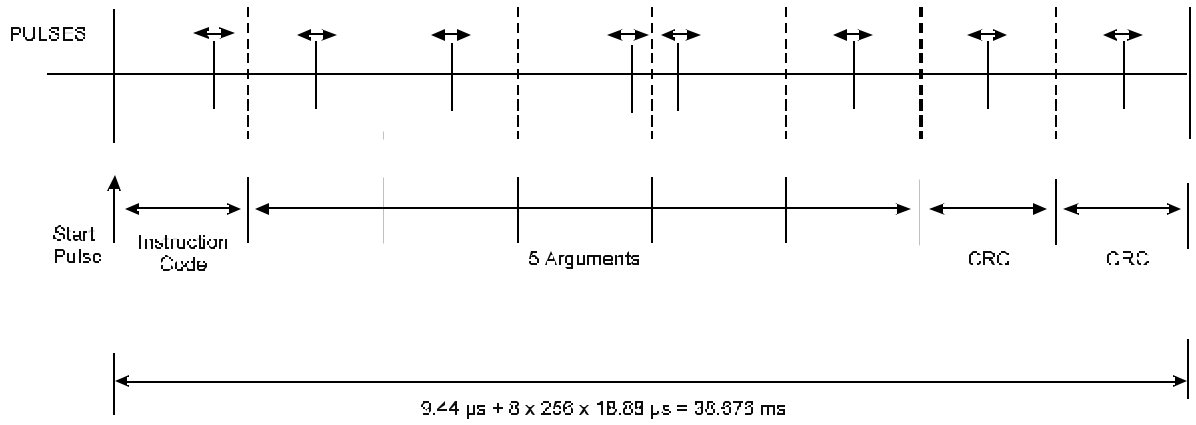
Each pulse in the command and QUIT frames (as described in the following sections) may have a maximum jitter of ±3.54 µs referred to the time determinant second edge of the start pulse (this is valid for standard mode and fast mode).

7.1 Command/Quit from Read/Write Device to I•CODE Label (RX)

7.1.1 Communication Frame 'COMMAND'

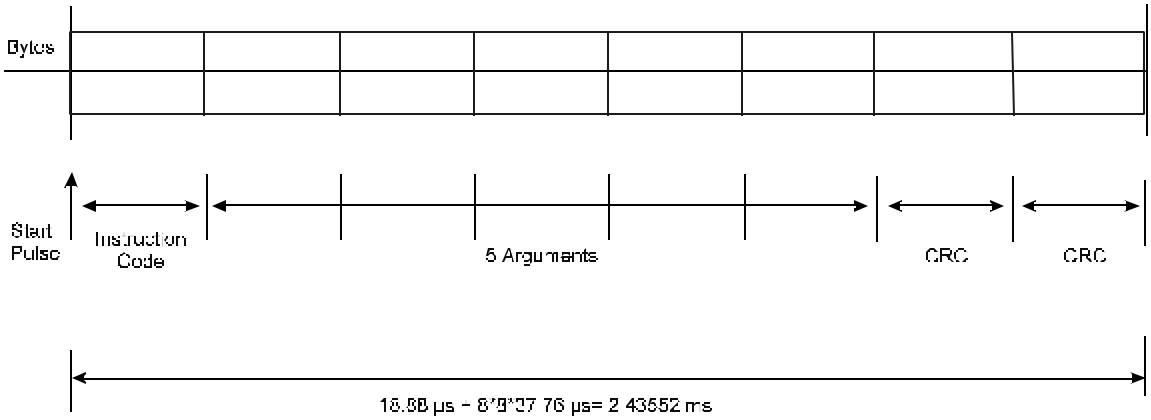
7.1.1.1 Standard Mode

Each COMMAND consists of a *standard start pulse* (9.44 µs modulation), followed by one '1 out of 256' instruction byte, five '1 out of 256' parameter bytes and two '1 out of 256' CRC bytes (16-bit CRC):



7.1.1.2 Fast Mode

Each COMMAND consists of a so-called *fast start pulse* (18.88 µs modulation), followed by one 8-bit instruction byte, five 8-bit parameter bytes and two CRC bytes (16-bit CRC):


Bytes
Start Pulse
Instruction Code
5 Arguments
CRC
CRC
18.88 µs * 8*9*37.76 µs= 2.43552 ms

7.1.2 Communication Frame 'QUIT'

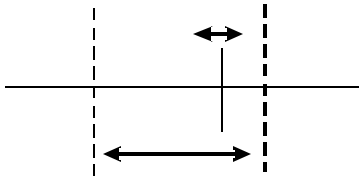
At the commands Anticollision/Select, Write and Halt an acknowledgement (for each timeslot) is necessary. This is done by the transmission of a byte in the QUIT frame.

At the above mentioned three commands each valid collision-free transmitted serial number of an I•CODE1 Label IC has to be acknowledged by a QUIT byte transmitted from the read/write device.

If a collision (or no response) is detected by the read/write device it transmits **no** pulse in the QUIT frame to the I•CODE1 Label IC.

7.1.2.1 Standard Mode

The QUIT frame at standard mode consists of one '1 out of 256' pulse (without start pulse):

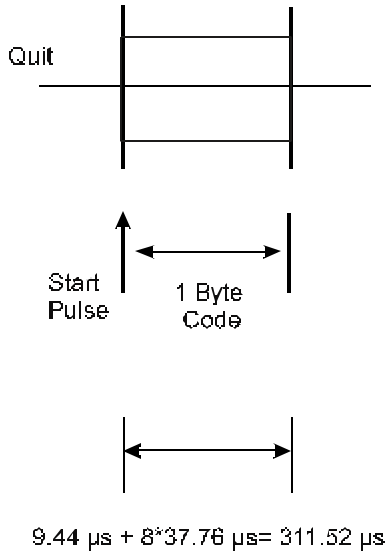


A QUIT value of zero is transmitted as pulse in (the last) position 256.

7.1.2.2 Fast Mode

The QUIT frame at fast mode consists of an 8-bit data byte (each bit frame = 37.76 µs) which is preceded by a start pulse (modulation with a duration of 9.44 µs).

The start pulse is necessary to distinguish a QUIT value of zero from the coding of 'no QUIT'.

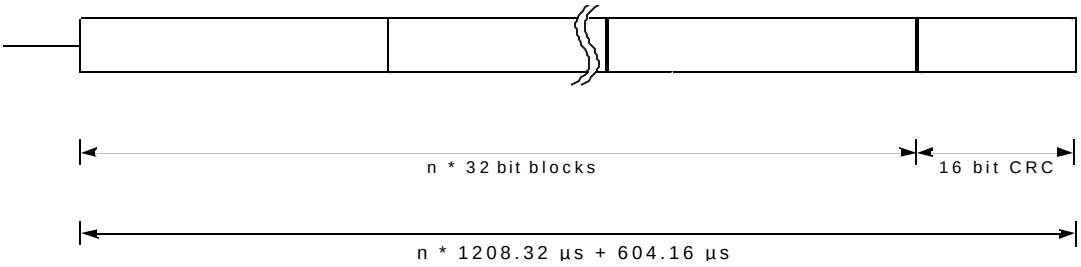


A QUIT value of zero is transmitted as start pulse (9.44 µs) and following 302.08 µs without modulation.

7.2 Response from I•CODE Label to Read/Write Device (TX)

7.2.1 Communication Frame 'RESPONSE'

Each 'RESPONSE' from the I•CODE1 Label IC consists of a multiple (n) of 32 bit blocks (content of addressed EEPROM blocks). The sequence is concluded by a 16 bit CRC. The response coding is the same for standard and fast mode.



7.2.2 Communication Frame 'EAS-RESPONSE'

For very long distance detection the I•CODE1 Label IC responses with a special (predefined) EAS sequence consisting of 256 bits (without CRC16). The duration of this special response is 9666.56 µs.

7.3 Minimum Time between Commands

At standard mode it is recommended to insert a delay of 5 ms between the end of the commands EAS, Read and Unselected Read (total time of each command see chapter 9) and the start pulse of the next command. This is to avoid situations where an I•CODE1 Label IC comes into the RF field immediately **after** the transmission of the start pulse and it can not synchronise to the next start pulse (for example if the next start pulse would be transmitted again by the read/write device immediately before the moment at which the I•CODE1 Label IC is ready to receive this start pulse). If there are situations at which any two consecutive pulses would be interpreted by the I•CODE1 Label IC as valid command (but of course the check of the CRC16 would identify this as no valid command) a delay of 39 ms instead of 5 ms is necessary to ensure the re-synchronisation to the start pulse of the next command.

At fast mode this delay is not necessary because the I•CODE1 Label IC can clearly distinguish between the (longer) start pulse for the fast mode and the other command pulses (with standard duration).

7.4 Optimisation of Modulation Pulse Duration

Due to different effects on the analogue parts of the read/write device (depending on antenna configuration, quality factor, ...) and the demodulator circuitry of the I•CODE1 Label IC the duration of the modulation pulses has to be optimised. The below given timing values refer to a digital signal which is generated in the read/write device and controls the modulation of the 13.56 MHz carrier.

For the current version of the I•CODE1 Label ICs a reduction of the duration of all modulation pulses from (nominal) 9.44 µs to 5.31 µs is recommended. Of course the complete bit frames have to keep their nominal duration (18.88 µs at standard mode and 37.76 µs at fast mode). The duration of the start pulse for the fast mode should be decreased from 18.88 µs to 17.11 µs.

The time determinant edge of each modulation pulse detected by the I•CODE1 Label IC is the **second** edge. Out of this the first edge should be delayed by 4.13 µs (at standard mode, 1.77 µs at fast mode) in order to reduce the pulse length (and with this keeping the second edge in the right time position).

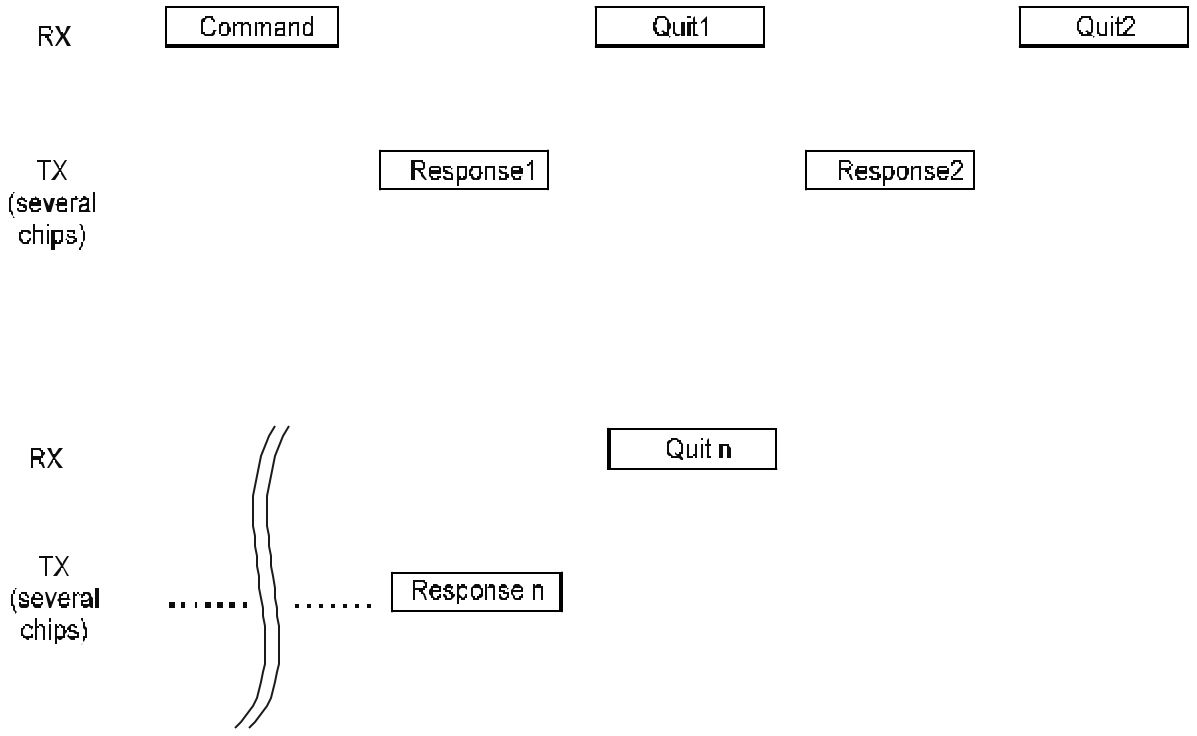
8 Communication Protocol

8.1 Basic Structure of the Protocol

The fulfilment of the strict requirements concerning the FCC limits is only possible if the number of modulations of the carrier on the read/write device is very low.

This can only be achieved with a *timeslot* based protocol, which means that each I•CODE1 Label IC responds in a chosen interval (timeslot) after the command received from the read/write device. The timeslot values are dependent on the serial number of the I•CODE1 Label ICs.

The following diagram shows the protocol structure in principle:



RX .... Command/acknowledgements transmitted from the read/write device to the I•CODE1 Label ICs
TX .... Response data transmitted from the I•CODE1 Label ICs to the read/write device

The number of possible timeslots to be used by the I•CODE1 Label ICs (1, 4, 8, 16, 32, 64, 128 or 256) is included as parameter in some commands from the read/write device (Anticollision/Select, Unselected Read).

Some other commands require a QUIT (acknowledgement) transmitted by the read/write device in order to be executed by the I•CODE1 Label IC (Anticollision/Select, Write, Halt).

8.2 Selection

If there are several I•CODE1 Label ICs in the antenna field it is necessary to decide which I•CODE1 Label IC should respond to a Read command, on which data should be written, ...

This choice is made by the *selection* of I•CODE1 Label ICs with the Anticollision/Select command. An I•CODE1 Label IC will remain in the timeslot chosen at the Anticollision/Select command for all further commands only if it gets a valid QUIT from the read/write device.

A selection of the I•CODE1 Label IC is necessary for valid execution of the following commands:

- Selected Read
- Write
- Halt

Once an I•CODE1 Label IC is selected it does not respond to the following commands:

- Anticollision/Select
- Unselected Read

The following commands work in selected as well as in unselected state:

- EAS
- Reset QUIET Bit

Even if an I•CODE1 Label IC is set into QUIET mode (by writing the bit pair 1|1 to bits 2 and 3 in block 3 of the EEPROM) it remains selected as long as it stays in the RF field.

8.3 Summary of I•CODE Commands

The I•CODE1 Label ICs support the following commands:

8.3.1 Anticollision/Select

At the Anticollision/Select command each of the **un**selected I•CODE1 Label ICs responds with its 64 bit serial number in different timeslots. Those I•CODE1 Label ICs which are alone in their timeslots are set into *selected* state by transmitting a QUIT byte from the read/write device to the I•CODE1 Label IC.

8.3.2 Selected Read

At the (Selected) Read command each of the **selected** I•CODE1 Label ICs responds with the given number of blocks (starting with the addressed block) in its timeslot at which the I•CODE1 Label IC was fixed with the Anticollision/Select command.

8.3.3 Unselected Read

At the Unselected Read command each of the **un**selected I•CODE1 Label ICs responds with the requested number of blocks (starting with the addressed block) in a **new** timeslot.

The difference to Selected Read is that the I•CODE1 Label ICs don't need to be selected to execute this command. This saves time if the serial number is not requested (but data of other memory blocks). This command does **not** select any I•CODE1 Label IC, therefore a Write or Halt command can only be used after Anticollision/Select.

Note: If there is more than one label in the field collisions can occur at each execution of the Unselected Read command (because each I•CODE1 Label IC always chooses a new timeslot at each Unselected Read command).

8.3.4 Write

At the Write command each of the **selected** I•CODE1 Label ICs responds with its 64 bit serial number (in its timeslot at which the I•CODE1 Label IC was fixed with the Anticollision/Select command) and the given 4 data bytes are written to the addressed block if the I•CODE1 Label ICs receives a QUIT from the read/write device in its timeslot.

8.3.5 Halt

At the Halt command each of the **selected** I•CODE1 Label ICs responds with its 64 bit serial number (in its timeslot at which the I•CODE1 Label IC was fixed with the Anticollision/Select command) and is set into HALT mode if the I•CODE1 Label IC receives a QUIT from the read/write device in its timeslot.

After this command the corresponding I•CODE1 Label ICs do not respond to any command until the next power-on reset (leaving and re-entering the RF field).

8.3.6 Reset QUIET Bit

If the two QUIET bits (bits 2 and 3 of block 3) are set to one (→ QUIET mode is enabled) the I•CODE1 Label IC does not respond to any command (with exception of the EAS command if the EAS mode is enabled), even if the label leaves and re-enters the antenna field (in contrast to the HALT mode, in that case the I•CODE1 Label IC is ready for the next command after re-entering the field).

The Reset QUIET Bit command clears the two QUIET bits of all I•CODE1 Label ICs which are in the antenna field and are in QUIET mode (independent of the current selection state and timeslot).

8.3.7 EAS

If both of the two EAS bits (bits 0 and 1 of block 3) are set the I•CODE1 Label IC responds with a special predefined EAS pattern (256 bits) at the execution of the EAS command.

The EAS command works in the unselected as well as in the selected state and is valid for all I•CODE1 Label ICs in the RF field and not restricted to a specific timeslot.

8.4 Optimum Number of Timeslots

Choosing too **few** timeslots compared to the number of I•CODE1 Label ICs in the field results in a lot of collisions (two or more labels respond in the same timeslot) and with this only a small number of labels can be selected.

In the case of choosing too **many** timeslots only few collisions will appear and nearly all of the labels in the field can be selected. The disadvantage in that case is that this is very time-consuming.

Simulations have shown that the optimum number of timeslots is about **twice** the number of I•CODE1 Label ICs expected in the antenna field at the same time.

If it is not possible to have an estimation of how many I•CODE1 Label ICs are in the field, it can be started with a lower number of timeslots. If many collisions are detected from the read/write device the number of timeslots should be increased.

Another possibility would be to select (with an Anticollision/Select command) only a few I•CODE1 Label ICs (in those timeslots where no collision appeared), do all commands which should be performed and set them into HALT mode. At next the remaining I•CODE1 Label ICs can be selected (with reduced probability of collisions because now the number of responding I•CODE1 Label ICs is smaller), worked off and finally set into HALT mode. This sequence can be repeated until no I•CODE1 Label IC responds to an Anticollision/Select command.

8.5 Family Code and Application Identifier

The I•CODE system offers the feature to use (independently) Family Codes and/or Application Identifiers with the following commands:

- Anticollision/Select
- Unselected Read
- EAS

The concerned two bytes are located at the beginning of the User Data (block 4, bytes 0 and 1).

If the read/write device transmits a value of zero for the Family Code and the Application Identifier all the I•CODE1 Label ICs will respond to the command, otherwise only those with matching Family Codes and Application Identifiers will respond. This feature enables the creation of ‘label families’.

Family Code and Application Identifier are independent from each other. That means, if one of them is set to zero in the command only the second has to match, if both are different to zero both have to match.

8.6 Write Protection

Writing to a certain block is only possible if this block is not write protected by the corresponding write access bit pair in block 2.

If both concerned write access bits are not set to one the I•CODE1 Label IC does **not** respond to the Write command, thus no QUIT has to be generated by the read/write device. Without valid QUIT the I•CODE1 Label IC will not start the programming of the EEPROM.

8.7 Error Handling at Write Command

If during the write process an error occurs (for example too less energy to program the EEPROM) the I•CODE1 Label IC will automatically be deselected.

If a Read command after the Write command is performed this can be used to verify if the Write command was successful or not.

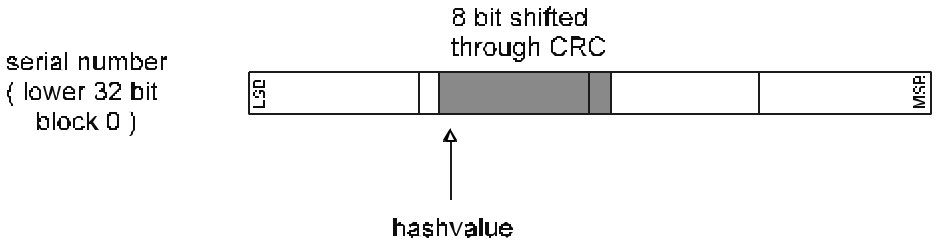
At all other errors (invalid CRC16, invalid QUIT or write attempts to write protected blocks) the I•CODE1 Label IC will remain in the selected state.

8.8 Calculation of Timeslot with Hashvalue

The calculation of the timeslot is done by the I•CODE1 Label IC with the help of a pointer, called *hashvalue*, which is included in the commands Anticollision/Select and Unselected Read. The calculated timeslot is stored in a register called timeslot register. After a selection of the I•CODE1 Label IC with an Anticollision/Select command (including a valid QUIT) the content of the timeslot register is fixed.

The timeslot register is pre-set with 01 hex only at power-on reset and not re-set at any time afterwards.

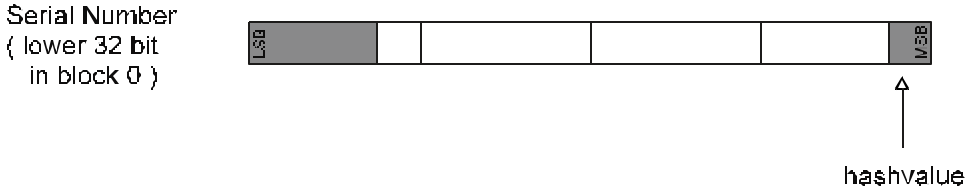
The hashvalue can be considered as bit address, pointing to the first of eight consecutive bits inside the unique serial number in block 0 (beginning with the LSB).



In this example the hashvalue is 9.

For calculation of the timeslot a CRC8 register (polynomial $x^8 + x^4 + x^3 + x^2 + 1$) is pre-set with the content of the timeslot register. Then 8 bits of the serial number beginning with the bit addressed by the hashvalue are shifted through the CRC8.

If the MSB of block 0 has been reached or exceeded (hashvalue is in the range 25 to 31) the calculation is finished with the lower bits of block 0 (‘wrap-around’).



In this example the hashvalue is 1E hex (30 decimal).

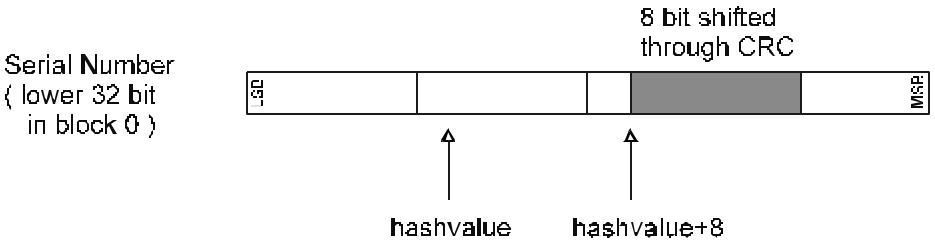
If there are fewer than 256 timeslots only the corresponding number of bits beginning with the LSB of the CRC8 are used as result for the timeslot. Always all 8 bits in the CRC8 are used internally for the next timeslot calculation.

For randomly distributed serial numbers it is the best way to start with a hashvalue of 0 and to increase this value at each additional Anticollision/Select command by 8. After having reached 24 the next starting value can be 4 (incremented by 8 again for each further Anticollision/Select command). Having reached 28, the next starting value can be 2 (incremented by 8 again for each further Anticollision/Select command) ...

8.9 Calculation of QUIT Value

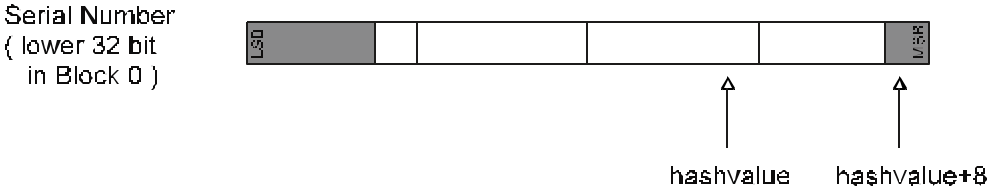
For generating the QUIT value at the Anticollision/Select, the Write and the Halt command, the pre-set value of the CRC8 register (polynomial $x^8 + x^4 + x^3 + x^2 + 1$) is a constant (FF hex). Then 8 bits of the serial number in block 0 are shifted through the CRC8. The first of these eight bits is addressed by **hashvalue + 8**.

Only if the result calculated by the I•CODE1 Label IC matches with the QUIT byte transmitted from the read/write device to the I•CODE1 Label IC the concerned command will be executed by the I•CODE1 Label IC (i.e. setting into selected state at the Anticollision/Select command, programming of the EEPROM at the Write command and setting into HALT mode at the Halt command, respectively).



In this example the hashvalue is 9.

If the MSB of block 0 has been reached or exceeded (hashvalue is in the range 17 to 23) the calculation is finished with the lower bits of block 0 ('wrap-around').



In this example the hashvalue is 16 hex (22 decimal).

Note: It is recommended to use different hashvalues at the Write command (and also at the Halt command) compared to that used at the Anticollision/Select command (for example 0 at AC/S, 8 at Write and 16 at Halt; that means, an offset of 8 or 16 at the hashvalue of each command following AC/S should be used).

8.10 Calculation of 16 bit CRC (Command/Response)

For the calculation of the 16 bit CRC the same generator polynomial ($x^{16} + x^{12} + x^5 + 1$) and also the same pre-set value (FFFE hex) are used for transmitting the command from the read/write device to the I•CODE1 Label IC as well as for the response of the I•CODE1 Label IC.

The start pulse of the command is **not** shifted through the CRC16. The transmission of the CRC16 always starts with the LSB.

The CRC16 can be calculated for the command and checked for the response (see the marked differences in the comment of the C-source) as described in the following example:

8.10.1 CRC16 Calculation Algorithm (C-Example)

```
#define  CRC_POLYNOM  0x8408
#define  CRC_PRESET   0xFFFE

unsigned int crc = CRC_PRESET;
int i, j, cnt = 6;               /* Command:  cnt = 6; */
                                 /* Response: cnt = 4 * number_of_blocks + 2; */
for (i = 0; i < cnt; i++)
{
    crc ^= Data[i];
    for (j = 0; j < 8; j++)
    {
        if (crc & 0x0001)
            crc = (crc >> 1) ^ CRC_POLYNOM;
        else
            crc = (crc >> 1);
    }
}

/* Command: */
Data[i]   = crc & 0xFF;          /* CRC16 low byte  */
Data[i+1] = crc >> 8;            /* CRC16 high byte */

/* Response: */
if (crc == 0)
    /* CRC calculation of response OK! */
else
    /* CRC error occurred! */
```

The variable `crc` is set to the pre-set value before each transmission of a command from the read/write device and before each response from the I•CODE1 Label IC.

8.11 Typical Sequence of Commands

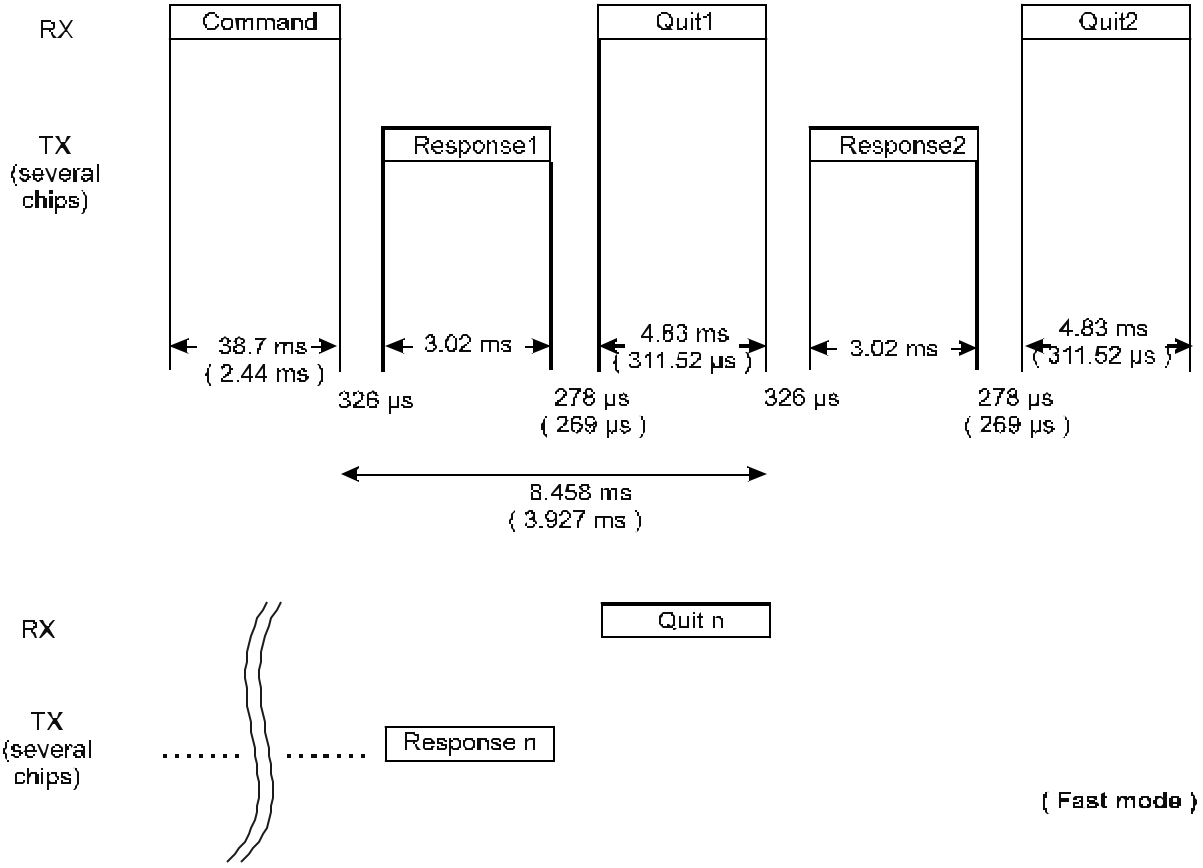
Because this matter is application dependent the below shown sequence can only be an example:

- Anticollision/Select (can be repeated with the same or different hashvalues)
- Read blocks
- Write block
- Read block (verifying the Write command)
- Halt
- :
- Anticollision/Select (can be repeated with the same or different hashvalues)
- Read blocks
- Write block
- Read block (verifying the Write command)
- Halt
- :

9 Command Frames (Timings/Parameters)

In the following timing diagrams all figures enclosed with brackets are valid for the fast mode, all other figures without brackets refer to the standard mode. Each instruction byte at Anticollision/Select, Unselected Read, Write and Halt is the sum of the corresponding instruction code and the hashvalue.

9.1 Anticollision/Select



RX command: Instruction code = 20 hex + hashvalue (0 ... 31) → (20 ... 3F hex)
Parameter byte 1 = 00 hex or Family Code (1 ... 255)
Parameter byte 2 = 00 hex or Application Identifier (1 ... 255)
Parameter byte 3 = z: exponent of number of timeslots (0 ... 7),
n: number of timeslots = 2^{z+1} (except for z = 0 → n = 1)
Parameter byte 4 = 00 hex
Parameter byte 5 = 00 hex
2 CRC16 bytes

TX response: 64 bit SNR, 16 bit CRC

RX quit: 1 byte depending on the serial number of the I•CODE1 Label IC and the hashvalue

Total time [µs] (n = number of timeslots)

Standard mode: 9.44 + 38666.24 + n * (325.68 + 3020.8 + 278.48 + 4833.28) = 38675.68 + n * 8458.24 µs

Fast mode: 18.88 + 2416.64 + n * (325.68 + 3020.8 + 269.04 + 311.52) = 2435.52 + n * 3927.04 µs

If an I•CODE1 Label IC has detected a valid QUIT byte after the transmission of its response all following read/write operations are fixed within this specific timeslot for this I•CODE1 Label IC.

The Anticollision/Select command can be repeated several times until no additional I•CODE1 Label IC responses or a sufficient number of occupied timeslots has been reached.

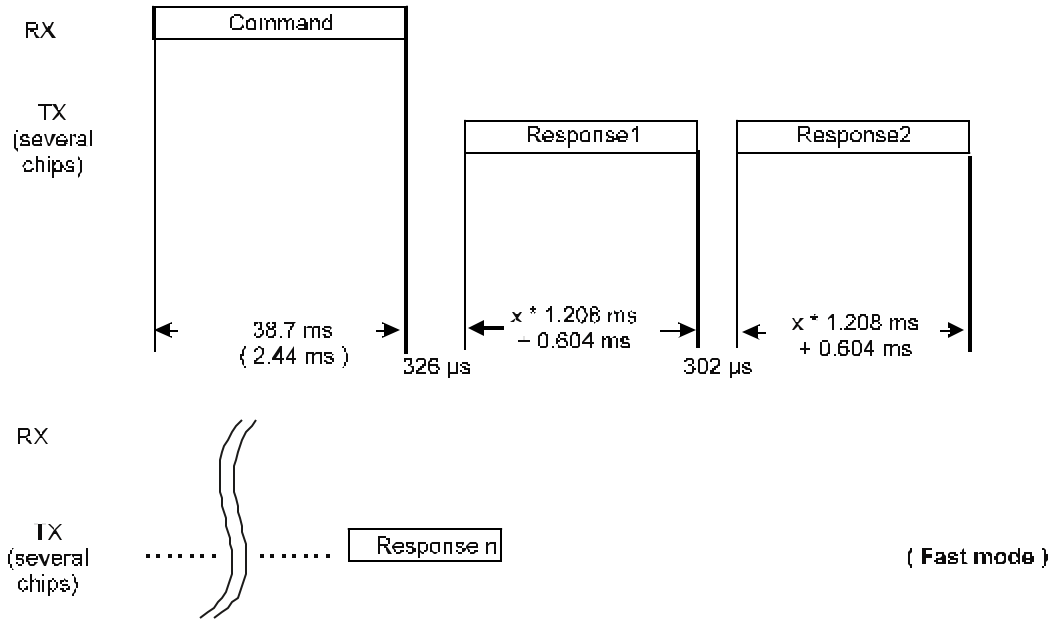
A selected I•CODE1 Label IC remains selected and will not respond to any further Anticollision/Select command until it leaves (and re-enters) the RF field.

Possible number of timeslots: 1, 4, 8, 16, 32, 64, 128, 256 (corresponding to z = 0 ... 7)

Parameter byte 1 must have the value zero if the Family Code should be ignored by the I•CODE1 Label IC. The same is valid for the Application Identifier with parameter byte 2.

9.2 Read x Blocks beginning with Block y

9.2.1 Selected Read



RX command: Instruction code = E1 hex
Parameter byte 1 = 00 hex
Parameter byte 2 = 00 hex
Parameter byte 3 = 00 hex
Parameter byte 4 = x – 1: number of blocks, decreased by one (x – 1 = 0 ... 15)
Parameter byte 5 = y: block address (0 ... 15)
2 CRC16 bytes

TX response: Data bits of x blocks, 16 bit CRC

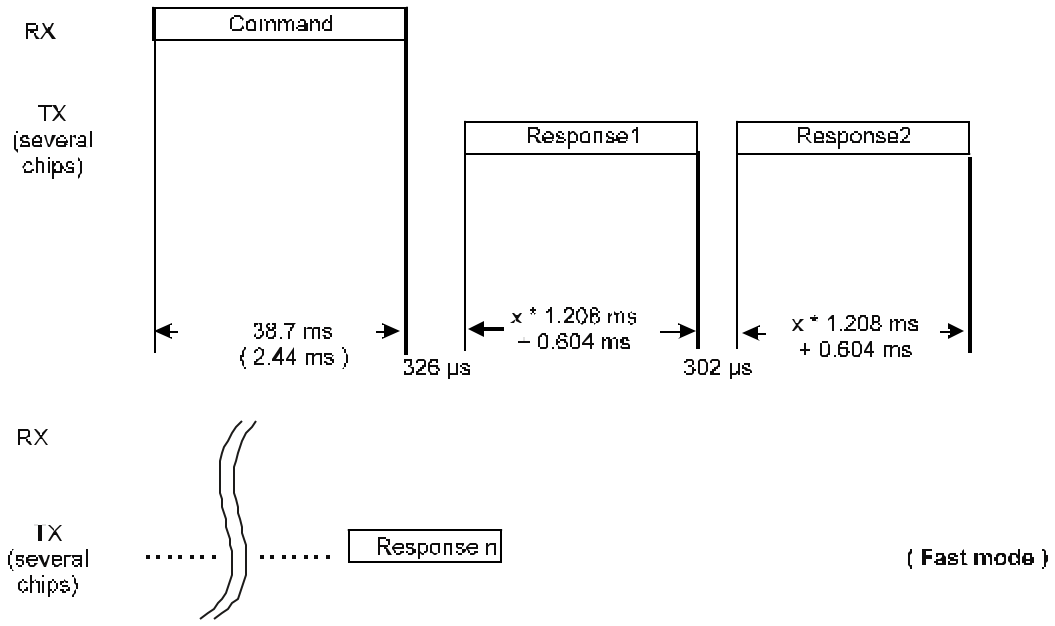
RX quit: None

Total time [µs] (n = number of timeslots, x = number of blocks)

Standard mode: 9.44 + 38666.24 + 325.68 + n * (x * 1208.32 + 604.16 + 302.08) = 39001.36 + n * (x * 1208.32 + 906.24) µs

Fast mode: 18.88 + 2416.64 + 325.68 + n * (x * 1208.32 + 604.16 + 302.08) = 2761.20 + n * (x * 1208.32 + 906.24) µs

9.2.2 Unselected Read



RX command: Instruction code = 40 hex + hashvalue (0 ... 31) → (40 ... 5F hex)
Parameter byte 1 = 00 hex or Family Code (1 ... 255)
Parameter byte 2 = 00 hex or Application Identifier (1 ... 255)
Parameter byte 3 = z: exponent of number of timeslots (0 ... 7),
n: number of timeslots = 2^{z+1} (except for z = 0 → n = 1)
Parameter byte 4 = x – 1: number of blocks, decreased by one (x – 1 = 0 ... 15)
Parameter byte 5 = y: block address (0 ... 15)
2 CRC16 bytes

TX response: Data bits of x blocks, 16 bit CRC

RX quit: None

Total time [µs] (n = number of timeslots, x = number of blocks)

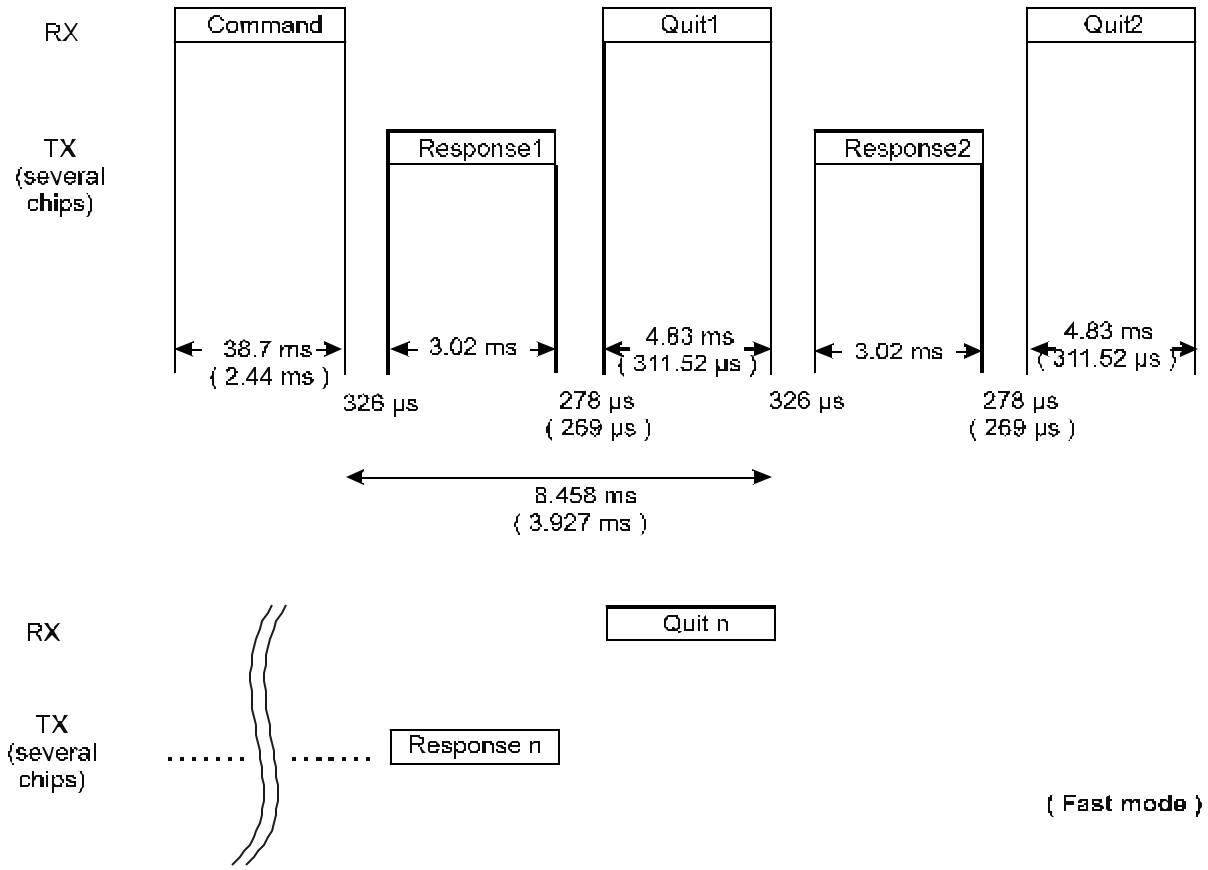
Standard mode: 9.44 + 38666.24 + 325.68 + n * (x * 1208.32 + 604.16 + 302.08) =
39001.36 + n * (x * 1208.32 + 906.24) µs

Fast mode: 18.88 + 2416.64 + 325.68 + n * (x * 1208.32 + 604.16 + 302.08) =
2761.20 + n * (x * 1208.32 + 906.24) µs

Possible number of timeslots: 1, 4, 8, 16, 32, 64, 128, 256

Parameter byte 1 must have the value zero if the Family Code should be ignored by the I•CODE1 Label IC. The same is valid for the Application Identifier with parameter byte 2.

9.3 Write Block x



RX command: Instruction code = 60 hex + hashvalue (0 ... 31) → (60 ... 7F hex)
Parameter byte 1 = data byte 0 (0 ... 255)
Parameter byte 2 = data byte 1 (0 ... 255)
Parameter byte 3 = data byte 2 (0 ... 255)
Parameter byte 4 = data byte 3 (0 ... 255)
Parameter byte 5 = x: block address (0 ... 15)
2 CRC16 bytes

TX response: 64 bit SNR, 16 bit CRC (or nothing if addressed block is already write-protected)

RX quit: 1 byte depending on the serial number of the I•CODE1 Label IC and the hashvalue

Total time [µs] (n = number of timeslots)

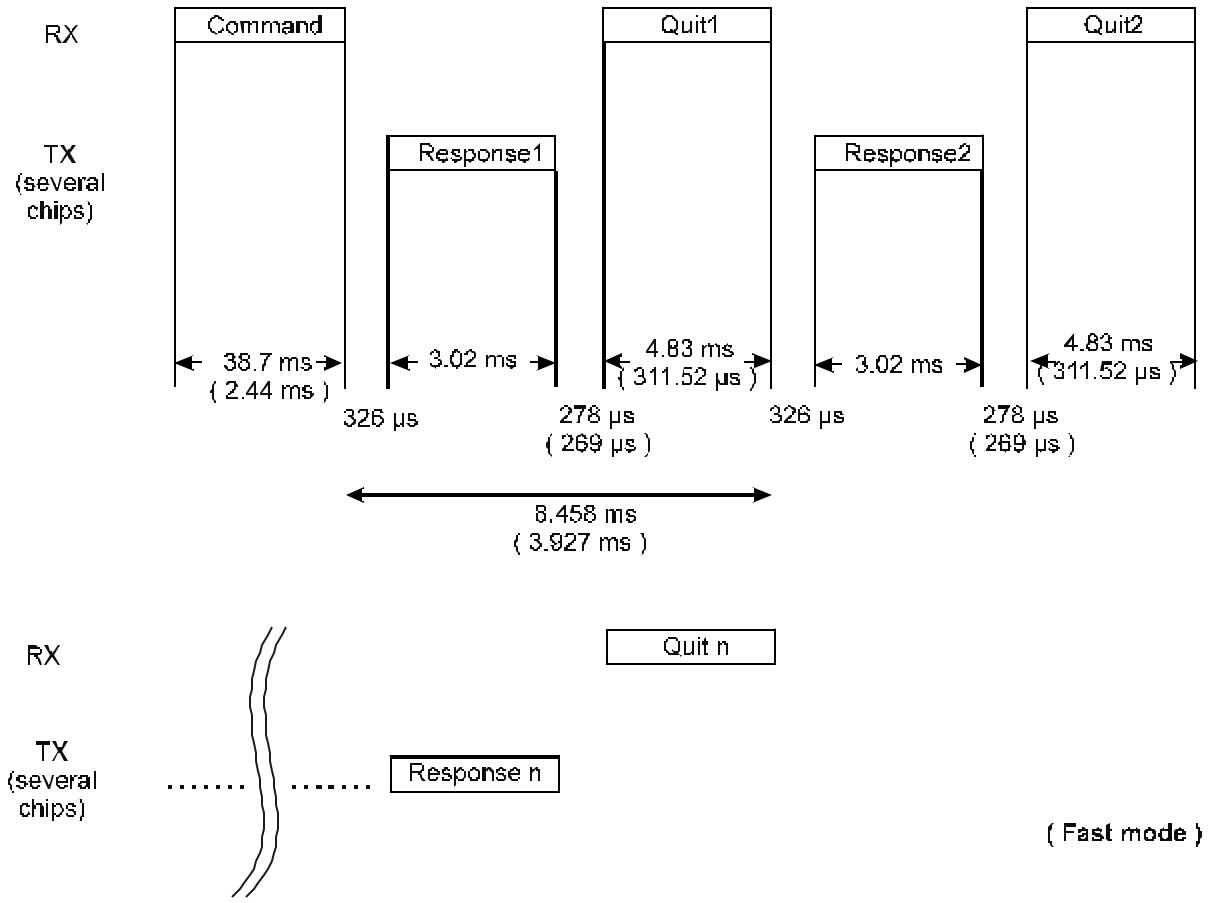
Standard mode: 9.44 + 38666.24 + n * (325.68 + 3020.8 + 278.48 + 4833.28) + 4852.16 = 43527.84 + n * 8458.24 µs

Fast mode: 18.88 + 2416.64 + n * (325.68 + 3020.8 + 269.04 + 311.52) + 4852.16 = 7287.68 + n * 3927.04 µs

Due to EEPROM programming in the I•CODE1 Label IC a minimum delay time of 4852.16 µs (included in 'total time') is required before the starting of a new command or switching off the RF.

The two EAS bits can be set or cleared with this command. The two QUIET bits can only be set with this command.

9.4 Halt



RX command: Instruction code = 80 hex + hashvalue (0 ... 31) → (80 ... 9F hex)
Parameter byte 1 = 00 hex
Parameter byte 2 = 00 hex
Parameter byte 3 = 00 hex
Parameter byte 4 = 00 hex
Parameter byte 5 = 00 hex
2 CRC16 bytes

TX response: 64 bit SNR, 16 bit CRC

RX quit: 1 byte depending on the serial number of the I•CODE1 Label IC and the hashvalue

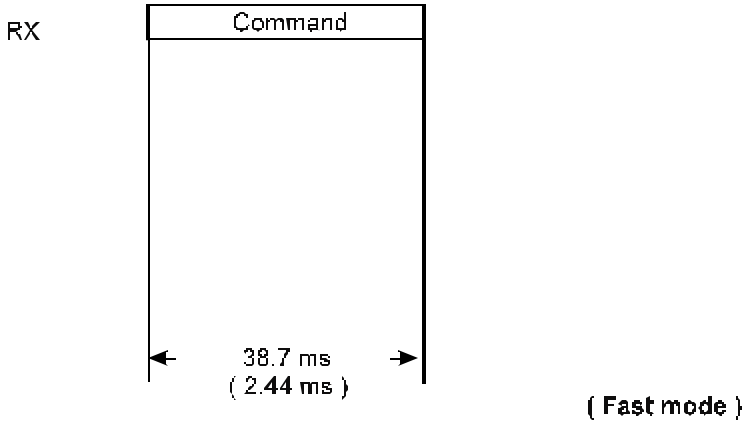
Total time [µs] (n = number of timeslots)

Standard mode: 9.44 + 38666.24 + n * (325.68 + 3020.8 + 278.48 + 4833.28) = 38675.68 + n * 8458.24 µs

Fast mode: 18.88 + 2416.64 + n * (325.68 + 3020.8 + 269.04 + 311.52) = 2435.52 + n * 3927.04 µs

If an I•CODE1 Label IC is set into HALT mode it does not respond to any command until the next power-on reset (e.g. leaving and re-entering the antenna field or switching off and on the RF).

9.5 Reset QUIET Bit



RX command: Instruction code = E2 hex
Parameter byte 1 = 00 hex
Parameter byte 2 = 00 hex
Parameter byte 3 = 00 hex
Parameter byte 4 = 00 hex
Parameter byte 5 = 00 hex
2 CRC16 bytes

TX response: None

RX quit: None

Total time [µs]

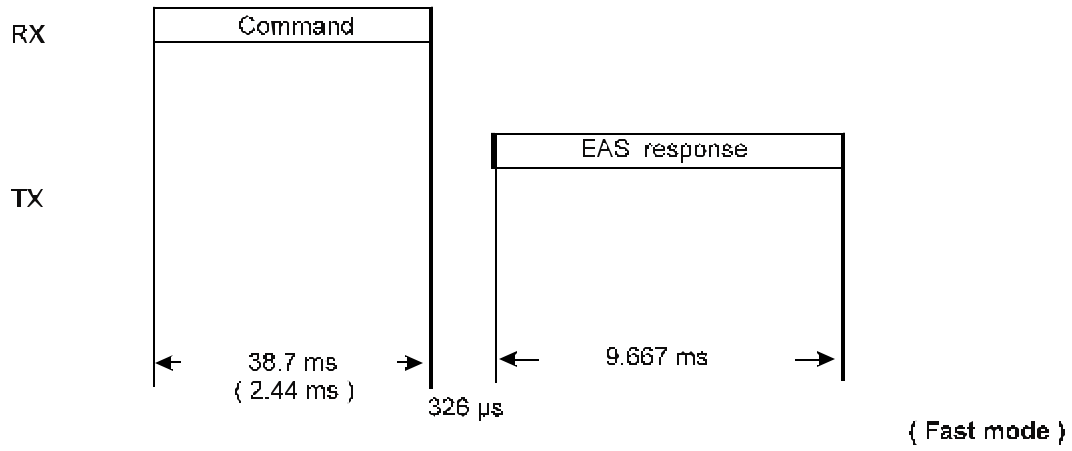
Standard mode: 9.44 + 38666.24 + 5154.24 = 43829.92 µs

Fast mode: 18.88 + 2416.64 + 5154.24 = 7589.76 µs

Due to EEPROM programming in the I•CODE1 Label IC a minimum delay time of 5154.24 µs (included in 'total time') is required before the starting of a new command or switching off the RF.

The QUIET bits are cleared for all I•CODE1 Label ICs in the field which are in QUIET mode. These bits can only be set by a normal Write command to block 3.

9.6 EAS



RX command: Instruction code = E0 hex
Parameter byte 1 = 00 hex or Family Code (1 ... 255)
Parameter byte 2 = 00 hex or Application Identifier (1 ... 255)
Parameter byte 3 = 00 hex
Parameter byte 4 = 00 hex
Parameter byte 5 = 00 hex
2 CRC16 bytes

TX response: 256 bit special EAS response

RX quit: None

Total time [µs]

Standard mode: 9.44 + 38666.24 + 325.68 + 256 * 37.76 = 48667.92 µs

Fast mode: 18.88 + 2416.64 + 325.68 + 256 * 37.76 = 12427.76 µs

EAS response (starting with the LSB, which is transmitted first; read from left to right):

11110100 11001101 01000110 00001110 10101011 11100101 00001001 11111110
00010111 10001101 00000001 00011100 01001011 10000001 10010010 01101110
01000001 01011011 01011001 01100001 11110110 11110101 11010001 00001101
10001111 00111001 10001011 01001000 10100101 01001110 11101100 11110111

The corresponding 32 bytes in hexadecimal notation are (as they are received by the read/write device):

2F	B3	62	70	D5	A7	90	7F
E8	B1	80	38	D2	81	49	76
82	DA	9A	86	6F	AF	8B	B0
F1	9C	D1	12	A5	72	37	EF

The calculation of these 256 bits is done using the same CRC8 generator polynomial ($x^8 + x^4 + x^3 + x^2 + 1$) as it is used for the timeslot and QUIT value calculation with the following conditions: the CRC8 pre-set value is FF hex and all 256 CRC8 input bits are set to zero.

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